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REMARKS

This application has been carefully reviewed in light of the Office Action dated April 30, 2002. Claims 11, 15, 16, 25, 27, 28, 30, 31, and 32 have been amended. A marked-up version of these claims, showing changes made, is attached hereto as Appendix A. Claims 12, 18, 20-24, and 26 have been canceled without prejudice or disclaimer to the subject matter recited therein. Applicant reserves the right to pursue the original claims and other claims in this application and in other applications. No new matter has been introduced. Claims 1, 3-10, 11, 13-17, 25, 27-32, and 39 are now pending in this application. Reconsideration of the above-referenced application in light of the amendments and following remarks is requested.

Claims 1, 3-4, 9-10, 18, and 22-24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fig. 11 of Chiang et al. (U.S. Patent No. 5,739,579) ("Chiang") in view of Fig. 9 of Chiang. Claims 18 and 22-24 have been canceled. Reconsideration is respectfully requested.

Claim 1 recites a semiconductor structure comprising "an insulator layer, a conductive plug . . . formed of a single conductive material, a doped region . . . an etch-stop layer located on said insulator layer and surrounding said plug, a non-conductive layer having an etched via at least partially over said conductive plug, and a conductive connector . . . including a first conductive layer . . . in contact with said etched via and a second conductive layer . . . in contact with said first conductive layer." (emphasis added).

The subject matter of claim 1 is not taught or suggested by Chiang. Chiang discloses a method of forming interconnect channels within a semiconductor device. The semiconductor device of Chiang includes a conductive plug, formed of a layer of titanium nitride 40 surrounding a tungsten layer 41, within a BPSG layer 22, an etch-stop layer 23, a barrier layer 60 and a metal layer 61. The barrier layer 60 and metal layer 61 fit within an interconnect channel 51, which is shown as an opening having a single diameter. Additional interconnect channels are shown, such as opening 330 (FIG. 16), opening 353

(FIG. 20), and interconnect channel 351 (FIGS. 21, 22), all of which are openings possessing a single diameter.

As the Office Action indicates, "Chiang does not teach the conductive connector includes a first conductor layer and a second conductor layer." (emphasis added) (Office Action, page 2). However, the Office Action asserts that "it would have been obvious . . . to substitute aluminum of Chiang's device (Fig. 11) with well-known copper/barrier layer taught by Chiang (Fig. 9)." (Office Action, page 3). Applicant respectfully submits that Chiang teaches away from the present invention.

Chiang teaches that "[t]he aluminum interconnects are not encapsulated because aluminum does not diffuse into silicon dioxide as opposed to copper . . . [and] the line width of the aluminum interconnect . . . is greater than the line width of the copper interconnects." (emphasis added) (Col. 11, lines 40-48).

Admittedly, Figure 9 of Chiang teaches a titanium nitride barrier layer 60 and a copper metal layer 61. However, Chiang merely suggests that "the copper within the interconnects is encapsulated to prevent copper diffusion into a silicon dioxide layer." (emphasis added) (Col. 10, lines 9-11). There is no simply motivation to substitute a copper/barrier layer of Figure 9 with Figure 11. The tungsten plug itself in Figure 11 acts as a diffusion barrier between the aluminum interconnect and the doped region. A second conductor layer is not taught or suggested in the embodiment depicted by Chiang's Figure 11. Further, Chiang's barrier layer 60 is designed only to prevent copper from diffusing outwards rather than suggesting a second conductive layer as the present invention claims.

Accordingly, Chiang does not teach or suggest a "conductive plug . . . formed of a *single conductive material* . . . and a conductive connector . . . including a *first conductive layer* . . . and a *second conductive layer*" as recited in claims 1, 3-4, and 9-10 (emphasis added). Thus, withdrawal of the rejection of claims 1, 3-4, and 9-10 is respectfully solicited.

Claims 3-4, and 9-10 depend from and contain all of the limitations of claim 1. Accordingly, claims 3-4 and 9-10 are allowable for at least the reasons set forth above for allowance of claim 1.

Claims 5-6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiang in view of Wang et al. (U.S. Patent No. 6,184,128) ("Wang"). Reconsideration is respectfully requested. Claims 5-6 depend from and contain all of the limitations of claim 1. Accordingly, claims 5-6 are allowable for at least the reasons given above for allowance of claim 1.

Claims 7-8 and 20-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiang in view of Hong et al. (U.S. Patent No. 6,008,117) ("Hong"). Reconsideration is respectfully requested. Claims 7-8 depend from and contain all of the limitations of claim 1. Claims 20-21 have been canceled. Accordingly, claims 7-8 are allowable for at least the reasons given above for allowance of claim 1.

Claims 11, 17, 25, 27, 32, and 39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsuura (U.S. Patent No. 5,598,027). Reconsideration is respectfully requested.

Claim 11 has been amended to include the limitations of claim 12 reciting a conductive layer comprising a first and second conductive layer. Matsuura does not disclose or suggest this feature in any manner. As the Office Action indicates, "Matsuura does not teach the conductive layer comprising a first conductive layer in via and a second conductive layer." (emphasis added) (Office Action, page 7). In the Office Action, claim 12 (which has now been canceled) was rejected over a combination of Matsuura and Chiang. However, as discussed above, Chiang does not disclose or suggest (and in fact, teaches away from) a structure with two conductive layers over a plug formed of a single conductive element.

Thus, amended claim 11 recites a semiconductor device comprising "at least one memory cell comprising an active region . . . a conductive plug formed of a single conductive material positioned . . . over said active region . . . being electrically connected with said active region, an etch-stop layer . . . an intermediate non-conductive layer provided over said etch-stop layer and having at least a first and second etched via over said plug . . . wherein said second etched via is above and has a greater diameter than said first etched via, and a first conductive layer formed in said first and second vias . . . and a second conductive layer." (emphasis added).

Similarly, claim 25 has been amended to emphasize that the conductive layer has a first conductive layer and a second conductive layer in contact with a conductive plug formed of a single element. Accordingly, amended claim 25 recites a processor-based system comprising "a processing unit, a semiconductor circuit coupled to said processing unit, said semiconductor circuit comprising a conductive plug formed of a single conductive material . . . provided on a connection region . . . an etch-stop layer . . . being at the same level as a top portion of said conductive plug . . . an intermediate non-conductive layer provided over said etch-stop layer and having at least a first and a second etched via over said conductive plug, wherein said second etched via is above and has a greater diameter than said first etched via, and a conductive connector electrically coupled to said connection region . . . comprising a first conductive layer deposited in and in contact with said first and second etched vias . . . including a portion in contact with said conductive plug, and a second conductive layer deposited over said first conductive layer." (emphasis added).

The Matsuura reference recites a semiconductor device with a substrate 1, a first interlayer insulating film 2, a first interconnection layer 4, a first etching prevention film 3, a second interlayer insulating film 5, a second interconnection layer 7, and a second etching prevention film 6. Matsuura fails to disclose or suggest the subject matter of amended claims 11 and 25.

Thus, withdrawal of the rejection of claims 11, 17, 25, 27, 32, and 39 is respectfully solicited.

Claim 17 depends from and contains all of the limitations of amended claim 11, and claims 27, 32, and 39 depend from and contain all of the limitations of amended claim 25. Accordingly, claim 17 is allowable for at least the reasons set forth above for allowance of amended claim 11, and claims 27, 32, and 39 are allowable for at least the reasons set forth above for allowance of claim amended claim 25.

Claims 13-14 and 28-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsuura in view of Hong. Reconsideration is respectfully requested. Claims 13-14 depend from and contain all of the limitations of amended claim 11. Similarly, claims 28-29 depend from and contain all of the limitations of amended claim 25. Accordingly, claims 13-14 and claims 28-29 are allowable for at least the reasons given above for allowance of amended claims 11 and 25.

Claims 12, 15-16, 26, and 30-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsuura in view of Chiang. Reconsideration is respectfully requested. Claims 12 and 15-16 depend from and contain all of the limitations of amended claim 11. Similarly, claims 26 and 30-31 depend from and contain all of the limitations of amended claim 25. Accordingly, claims 12, 15-16, 26, and 30-31 are allowable for at least the reasons given above for allowance of amended claims 11 and 25.

As discussed previously, Chiang fails to remedy the deficiency found in the Matsuura reference. Further, Chiang discloses interconnect channels such as opening 330 (FIG. 16), opening 353 (FIG. 20), and interconnect channel 351 (FIGS. 21, 22), all of which are openings possessing a single diameter. Matsuura provides vias B and C as Figure 1 illustrates possessing different diameters. There simply is no motivation to combine Chiang with Matsuura. Accordingly, this is an additional reason for withdrawal of the rejections regarding claims 12, 15-16, 26, and 30-31.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By _____

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APPENDIX A

11. (Twice Amended) A semiconductor device comprising:

at least one memory cell comprising:

an active region in a substrate;

a conductive plug formed of a single conductive material positioned within an insulator layer and provided over said active region, said conductive plug being electrically connected with said active region;

an etch-stop layer deposited on said insulator and around said conductive plug;

an intermediate non-conductive layer provided over said etch stop layer and having at least a first and a second etched via over said plug, wherein said second etched via is above and has a greater diameter than said first etched via; and

[at least one conductive layer in said first and second vias in electrical connection with said plug], a first conductive layer deposited in and in contact with said first and second vias, said first conductive layer including a portion in contact with said conductive plug, and a second conductive layer deposited over and in contact with said first conductive layer.

15. (Amended) The semiconductor memory device of claim [12] 11, wherein said first conductive layer comprises one or more materials selected from the group consisting of

aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

16. (Amended) The semiconductor memory device of claim [12] 11, wherein said second conductive layer comprises one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, titanium, titanium nitride and tungsten.

25. (Twice Amended) A processor-based system comprising:

a processing unit;

a semiconductor circuit coupled to said processing unit, said semiconductor circuit comprising:

a conductive plug formed of a single conductive material positioned within an insulator and provided on a connection region;

an etch-stop layer deposited on said insulator, said etch-stop layer being at the same level as a top portion of said conductive plug;

an intermediate non-conductive layer provided over said etch-stop layer and having at least a first and a second etched via over said conductive plug, wherein said second etched via is above and has a greater diameter than said first etched via; and

a conductive connector electrically coupled to said connection region, said conductive connector comprising a first conductive layer deposited in and in contact with said first and second etched vias, said first conductive layer including a portion in

contact with said conductive plug, and a second conductive layer deposited over and in contact with said first conductive layer.

27. (Amended) The processor-based system of claim [26] 25, wherein said connection region comprises a doped region within said substrate.

28. (Amended) The processor-based system of claim [26] 25, wherein said intermediate layer comprises doped silicate glass.

30. (Amended) The processor-based system of claim [26] 25, wherein said first conductive layer comprises at least one layer of one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

31. (Amended) The processor-based system of claim [26] 25, wherein said second conductive layer comprises at least one layer of one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

32. (Amended) The processor-based system of claim [26] 25, further comprising a substrate, and wherein said connection region is located in said substrate, and wherein said conductive plug is located over said connection region.